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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/598,143	11/18/2009	Michael Bauer	I431.170.101/FIN561PCT/US	1554

25281 7590 04/27/2011

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EXAMINER	
ZISKIND, DAVID	

ART UNIT	PAPER NUMBER
2818	

MAIL DATE	DELIVERY MODE
04/27/2011	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/598,143	BAUER ET AL.	
	Examiner	Art Unit	
	David Ziskind	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 April 2010*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *24-46* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/18/2006* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *4/12/2010*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the reference numerals do not correlate with any numerals given in the specification. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they do not include the following reference sign(s) mentioned in the description: too many to list, but as an example, reference numeral “100” is nowhere to be found on the proposed drawings. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either “Replacement Sheet” or “New Sheet” pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be

notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. As a suggestion, it should be noted that the drawings in the German language WIPO Version of the instant application are completely different from those provided with the National Entry Stage application (and from this Examiner's limited knowledge of German), match more closely with the specification as provided.

Claim Objections

4. Claim 27 is objected to because of the following informalities: the limitation is grammatically incorrect. Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 24-27 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448).

In regards to claim 24, Coomer discloses a semiconductor component comprising: a stack of semiconductor chips (310), the semiconductor chips being

arranged in a manner fixed cohesively one on top of another (chips [310] are bonded together by a dielectric [fig. 5 **Step 510**], the semiconductor chips comprising contact areas (terminus of each conductor (410, 420) and conductor portions (410, 420) extending from at least one upper edge (fig. 4B discloses a conductor passing over an upper edge of device [440A]) to a lower edge of the edge sides of the semiconductor chips (fig. 4B discloses a conductor passing to the lower edge of device [440A] but above device [440B] and electrically connecting the contact areas of the semiconductor chips of the semiconductor chip stack ([440B and substrate (401) are electrically interconnected via conductors [430].) ([¶0021]

Coomer differs from the claimed invention in that it does not disclose contact areas extending as far as the edges of the semiconductor chips.

Figures 1 and 5 of Val et al. discloses contacts P.sub.E arranged on the front edge of a semiconductor plate, constituting a rewiring layer Col. 2, ll. 19-25.

It would have been obvious to modify the stack of Coomer to incorporate the edge contacts of Val et al. in order to shorten the length the conductor must travel.

In regards to claim 25, fig. 4B of Coomer discloses devices 440A and 440B being of different size.

In regards to claim 26, the combination does not disclose semiconductor chips having a different number of contact areas at their edges.

However, it would have been obvious to use semiconductor chips having a different number of contact areas at their edges in order to have latitude in the design of the chip stack.

In regards to claim 27, figs. 4B and 5 of Coomer disclose electrically conductive conductor portions arranged adhesively on the semiconductor chip edges (via dielectric), the semiconductor edge sides, the semiconductor top side and/or the semiconductor rear side. Moreover, Val et al. discloses the contacts P.sub.E on each semiconductor plate. Figures 6a-6b of Val et al. shows that each stack contact (P.sub.E) can be made by laser etching. Thus, each plate can be stacked "out of order" by switching the order of the plates prior to etching. Thus, Val et al. discloses a freely selectable stacking order.

In regards to claim 45, fig. 4B of Coomer discloses devices 440A and 440B being of different size. However, the combination does not disclose semiconductor chips having a different number of contact areas at their edges.

However, it would have been obvious to use semiconductor chips having a different number of contact areas at their edges in order to have latitude in the design of the chip stack.

7. Claim 28, 30, 32 and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007).

In regards to claim 28, the combined component differs from the claimed invention in that it does not disclose conductor portions comprise an adherent plastic resist which is filled with metallic nanoparticles and is electrically conductive.

Hubert et al. disclose a method of creating a wide variety of materials utilizing nanoparticles, such gold and silver nanoparticle inks. [¶0061]. Moreover, Hubert et al. disclose a clear adhesive pre-cursor (NORLAND optical adhesive #72.) In addition, Hubert et al. disclose the creation of conductive polymers, in addition to resists. [¶0061]. Thus, it is obvious to one of ordinary skill in the art, utilizing the teachings of Hubert et al. would be able to use his disclosure to create an electrically conductive adherent plastic resist filled with metallic particles.

It would have been obvious to use the teachings of Hubert et al. with the combined component in order to minimize the size of the wiring.

In regards to claim 30, Val et al. discloses **Step 64**, which deposits metal, M, on all of the faces of the stack. Afterwards, each of the connections C are formed by two etchings (51) and (52) with the help of a laser. Col. 3, ll. 18-23.

Val et al. differs from the claimed invention in that the metal M is not a resist.

However, Hubert et al. discloses a resist with an optical precursor (NORLAND #72).

It would have been obvious to use the method of Hubert et al. in the combination device because laser etching resist is a common practice in the formation of interconnects in semiconductors.

In regards to claim 32, Val et al. discloses a semiconductor chip stack (Fig. 1). Val also discloses a multilayer rewiring layer (the contacts P.sub.E can be rewired by a simple change of the etching parameters of contact C) (See figs. 5, 6a).

Val et al does not disclose a layer comprising nanopariticle-filled electrically conductive patterned plastic resist layers and insulation layers arranged in between on the edge sides of the semiconductor chips.

Hubert et al. disclose a method of creating a wide variety of materials utilizing nanoparticles, such gold and silver nanoparticle inks. [¶0061]. Moreover, Hubert et al. disclose a clear adhesive pre-cursor (NORLAND optical adhesive #72.) In addition, Hubert et al. disclose the creation of conductive polymers, in addition to resists. [¶0061]. Thus, it is obvious to one of ordinary skill in the art, utilizing the teachings of Hubert et al. would be able to use his disclosure to create an electrically conductive adherent plastic resist filled with metallic particles.

It would have been obvious to use the teachings of Hubert et al. with the combined component in order to minimize the size of the wiring.

Furthermore, Val et al. discloses conductive patterns arranged in between on the edge sides of the semiconductor chips. (Fig. 5).

It would have been obvious to modify the stack of Val et al. to incorporate the edge contacts of Hubert et al. in order to shorten the length the conductor must travel.

In regards to claim 42, Val et al. discloses **Step 64**, which deposits metal, M, on all of the faces of the stack. Afterwards, each of the connections C are formed by two etchings (51) and (52) with the help of a laser. Col. 3, ll. 18-23.

Val et al. differs from the claimed invention in that the metal M is not a resist.

However, Hubert et al. discloses a resist with an optical precursor (NORLAND #72).

It would have been obvious to use the method of Hubert et al. in the combination device because laser etching resist is a common practice in the formation of interconnects in semiconductors.

8. Claim 33 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007) and further in view of Chen et al. (2002/0105789).

In regards to claim 33, Coomer discloses a semiconductor component comprising: a stack of semiconductor chips (310), the semiconductor chips being arranged in a manner fixed cohesively one on top of another (chips [310] are bonded together by a dielectric [fig. 5 **Step 510**], the semiconductor chips comprising contact areas (terminus of each conductor (410, 420) and conductor portions (410, 420) extending from at least one upper edge (fig. 4B discloses a conductor passing over an upper edge of device [440A]) to a lower edge of the edge sides of the semiconductor chips (fig. 4B discloses a conductor passing to the lower edge of device [440A] but above device [440B] and electrically connecting the contact areas of the semiconductor chips of the semiconductor chip stack ([440B and substrate (401) are electrically interconnected via conductors [430].) ([¶0021]. Furthermore, Coomer discloses patterning a layer to form interconnect sections between the contact areas of the semiconductor chips stacked one on top of each other. (fig. 5)

However, Coomer differs from the claimed invention in that it does not disclose contact areas extending as far as the edges of the semiconductor chips.

Figures 1 and 5 of Val et al. discloses contacts P.sub.E arranged on the front edge of a semiconductor plate. Col. 2, ll. 19-25.

It would have been obvious to modify the stack of Coomer to incorporate the edge contacts of Val et al. in order to shorten the length the conductor must travel.

However, the combined device differs from the claimed invention in that it does disclose encapsulating the semiconductor stack with a layer of plastic resist which is filled with nanoparticles.

Hubert et al. disclose a method of creating a wide variety of materials utilizing nanoparticles, such gold and silver nanoparticle inks. [¶0061]. Moreover, Hubert et al. disclose a clear adhesive pre-cursor (NORLAND optical adhesive #72.) In addition, Hubert et al. disclose the creation of conductive polymers, in addition to resists. [¶0061]. Thus, it is obvious to one of ordinary skill in the art, utilizing the teachings of Hubert et al. would be able to use his disclosure to create an electrically conductive adherent plastic resist filled with metallic particles.

However, the combination method does not disclose a method that would encapsulate the semiconductor stack with a layer made of plastic resist filled with nanoparticles.

Chen et al. disclose an encapsulation of a chip stack which circumvents the outer part of the device.

Thus, it would have been obvious to use the teachings of Hubert et al. and Chen et al. with the combined component in order to minimize the size of the wiring.

9. Claim 29 and 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007) and further in view of the NORLAND data sheet (2/1998).

In regards to claim 29, NORLAND optical adhesive #72 is soluble until fully cured. See data sheet, p. 1.

It would have been obvious to use the NORLAND optical adhesive #72 in the combined device since it is important to use a soluble material when dealing with particles suspended in a resist.

In regards to claim 41, NORLAND optical adhesive #72 is soluble until fully cured. See data sheet, p. 1.

It would have been obvious to use the NORLAND optical adhesive #72 in the combined device since it is important to use a soluble material when dealing with particles suspended in a resist.

10. **Claims 31 and 43 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007) and further in view of the Choi et al. *A Photocurable Poly(dimethylsiloxane) Chemistry Designed for Soft Lithographic Molding and Printing in the Nanometer Regime* (hereinafter "Photocurable Chemistry")**

11. **In regards to claim 31,** the combined device differs from the claimed invention in that the nanoparticle-filled plastic resist is not patterned photolitographically.

Norland data sheet discloses that NORLAND #72 is UV curable.

Photocurable Chemistry discloses that NOA #72 may be used as a photocurable polyurethane (Fig. 2) to replicate uniform defect-free patterns on a silicon wafer.

It would have been obvious to use NORLAND #72 as a photoresist, as disclosed in Photocurable chemistry, because photoresist use is an extremely common practice in the formation of interconnects in semiconductors and performs well with nanotechnology.

In regards to claim 43, the combined device differs from the claimed invention in that the nanoparticle-filled plastic resist is not patterned photolitographically.

Norland data sheet discloses that NORLAND #72 is UV curable.

Photocurable Chemistry discloses that NOA #72 may be used as a photocurable polyurethane (Fig. 2) to replicate uniform defect-free patterns on a silicon wafer.

It would have been obvious to use NORLAND #72 as a photoresist, as disclosed in Photocurable chemistry, because photoresist use is an extremely common practice in the formation of interconnects in semiconductors and performs well with nanotechnology.

12. Claim 34 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) in view of Hubert et al. (2004/0026007) and further in view of Chen et al. (2002/0105789).

The combined method differs from the claimed invention in that it does not disclose a method of spraying on the layer made of plastic resist for encapsulating the semiconductor stack.

Fig. 4. of Chen et al discloses a method of providing a layer (41, 42) made of an encapsulant body for encapsulating the semiconductor stack. While not explicit, Chen et al. discloses substrate (13) may be a phenolyc resin. Thus, it would have been obvious to use a plastic resin as the encapsulant for the chip stack (11, 12).

Chen does not disclose a method of spraying on the layer made of resist. However, it would have been obvious to one of ordinary skill in the art to spray a layer of resist to encapsulate the chip stack in order to encapsulate the stack.

13. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007), Chen et al. (2002/0105789) and further in view of Derderian (2003/0038353).

The combined method differs from the claimed invention in that it does not disclose a method of dipping the semiconductor stack, for encapsulation with a layer made of plastic resist, into a bath of nanoparticle-filled plastic resist.

Fig.4 of Derderian (2003/0038353) discloses dipping at least portions of a chip stack in a dielectric. [¶ 0046].

It would have been obvious to dip at least portions of a chip stack in a dielectric material in order to evenly coat it.

However, Chen et al discloses a complete encapsulation of a semiconductor chip stack.

Hubert et al. discloses a method of creating a wide variety of materials utilizing nanoparticles, such gold and silver nanoparticle inks. [¶0061]. Moreover, Hubert et al. disclose a clear adhesive pre-cursor (NORLAND optical adhesive #72.) In addition, Hubert et al. disclose the creation of conductive polymers, in addition to resists. [¶0061]. Thus, it is obvious to one of ordinary skill in the art, utilizing the teachings of Hubert et al. would be able to use his disclosure to create an electrically conductive adherent plastic resist filled with metallic particles.

Thus, the combination of Chen and Hubert et al. would be obvious to include in the main device in order to ensure proper wiring between the chips in the stack.

14. Claim 36 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007), Chen et al. (2002/0105789) in view of Val (5,637,536) and further in view of Farnworth (7,060,526).

The combination device does not disclose a method effecting a laser removal method for patterning the nanoparticle-filled plastic resist to form interconnect sections

Farnworth discloses in fig. 3J, a resist layer (82) etched by a laser for patterning an interconnect section. (which may include nanoparitcles. See Col. 12, ll. 32-45.

It would have been obvious to use the method of Farnworth in the combined method in order to ensure the integrity of the connection.

15. Claim 37-38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007), Chen et al. (2002/0105789) in view of Val (5,637,536) and further in view of Farnworth (7,060,526) and further in view of *Photocurable Chemistry.*

In regards to claim 37, the combined method differs from the claimed invention in that the method to carry out a photolithography method for patterning the nanoparticle-filled made of plastic resist is to form interconnect sections.

Norland data sheet discloses that NORLAND #72 is UV curable.

Photocurable Chemistry discloses that NOA #72 may be used as a photocurable polyurethane (Fig. 2) to replicate uniform defect-free patterns on a silicon wafer.

It would have been obvious to use NORLAND #72 as a photoresist, because photoresist use is an extremely common practice in the formation of interconnects in semiconductors and performs well with nanotechnology.

Moreover, Farnworth connects the vias in the resist to the interconnect sections (28) in order to ensure device reliance.

In regard to claim 38, the combined method does not disclose a method of applying the interconnect sections to the semiconductor stack selectively by precision injection techniques. However, it would have been obvious to one of ordinary skill in the art to apply the interconnect sections to the semiconductor stack selectively by precision

injection techniques since it is a goal of packaging to create precise connections between the chips.

16. Claim 39 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007), Chen et al. (2002/0105789) in view of Val (5,637,536) and further in view of Farnworth (7,060,526) in view of *Photocurable Chemistry* and further in view of Nordal et al.

In regards to claim 39, the combined method differs from the claimed invention in that it does not disclose a method of applying multilayer interconnect sections in alternation with insulation layers to the semiconductor stack.

Figure 11b of Nordal et al. discloses an insulation layer IL1 between each semiconductor track.

It would have been obvious to combine Nordal et al. with the nano-conductor of Hubert et al. to alternate the devices within the stack in order to increase performance by reducing interference.

In regards to claim 44, the combined method differs from the claimed invention in that it does not disclose a multilayer wiring sections in alternation with insulation layers to the semiconductor stack.

Figures 1 and 5 of Val et al. discloses contacts P.sub.E arranged on the front edge of a semiconductor plate, constituting a rewiring layer Col. 2, ll. 19-25.

Hubert et al. discloses a method of creating a wide variety of materials utilizing nanoparticles, such gold and silver nanoparticle inks. [¶0061]. Moreover, Hubert et al. disclose a clear adhesive pre-cursor (NORLAND optical adhesive #72.) In addition, Hubert et al. disclose the creation of conductive polymers, in addition to resists. [¶0061]. Thus, it is obvious to one of ordinary skill in the art, utilizing the teachings of Hubert et al. would be able to use his disclosure to create an electrically conductive adherent plastic resist filled with metallic particles.

However, figure 11b of Nordal et al. discloses an insulation layer IL1 between each semiconductor track.

It would have been obvious to combine Nordal et al. with the nano-conductor of Hubert et al. to alternate the devices within the stack in order to increase performance by reducing interference.

17. **Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448) and further in view of Hubert et al. (2004/0026007).**

Coomer discloses a semiconductor component comprising: a stack of semiconductor chips (310), the semiconductor chips being arranged in a manner fixed cohesively one on top of another (chips [310] are bonded together by a dielectric [fig. 5 **Step 510**], the semiconductor chips comprising contact areas (terminus of each conductor (410, 420) and conductor portions (410, 420) extending from at least one upper edge (fig. 4B discloses a conductor passing over an upper edge of device [440A])

to a lower edge of the edge sides of the semiconductor chips (fig. 4B discloses a conductor passing to the lower edge of device [440A] but above device [440B] and electrically connecting the contact areas of the semiconductor chips of the semiconductor chip stack ([440B and substrate (401) are electrically interconnected via conductors [430].) ([¶0021]

Coomer differs from the claimed invention in that it does not disclose contact areas extending as far as the edges of the semiconductor chips.

Figures 1 and 5 of Val et al. discloses contacts P.sub.E arranged on the front edge of a semiconductor plate. Col. 2, ll. 19-25. Moreover, Val et al. discloses the contacts P.sub.E on each semiconductor plate. Figures 6a-6b of Val et al. shows that each stack contact (P.sub.E) can be made by laser etching. Thus, each plate can be stacked "out of order" by switching the order of the plates prior to etching. Thus, Val et al. discloses a freely selectable stacking order.

It would have been obvious to modify the stack of Coomer to incorporate the edge contacts of Val et al. in order to shorten the length the conductor must travel

Hubert et al. discloses a method of creating a wide variety of materials utilizing nanoparticles, such gold and silver nanoparticle inks. [¶0061]. Moreover, Hubert et al. disclose a clear adhesive pre-cursor (NORLAND optical adhesive #72.) In addition, Hubert et al. disclose the creation of conductive polymers, in addition to resists. [¶0061]. Thus, it is obvious to one of ordinary skill in the art, utilizing the teachings of Hubert et al. would be able to use his disclosure to create an electrically conductive adherent plastic resist filled with metallic particles.

It would have been obvious to add the teachings of Hubert et al. to the main device in order to ensure proper wiring between the chips in the stack.

18. Claims 46 is rejected under 35 U.S.C. 103(a) as being unpatentable over Coomer (2003/0132527) in view of Val et al. (5,847,448).

Claim 46 shall be interpreted under 35 USC 112 ¶ 6.

Coomer discloses a semiconductor component comprising: a stack of semiconductor chips (310), the semiconductor chips being arranged in a manner fixed cohesively one on top of another (chips [310] are bonded together by a dielectric [fig. 5 **Step 510**], the semiconductor chips comprising contact areas (conductors [410, 420]) Coomer differs from the claimed invention in that it does not disclose contact areas extending as far as the edges of the semiconductor chips.

Figures 1 and 5 of Val et al. discloses contacts P.sub.E arranged on the front edge of a semiconductor plate. Col. 2, ll. 19-25.

It would have been obvious to modify the stack of Coomer to incorporate the edge contacts of Val et al. in order to shorten the length the conductor must travel.

According to 35 USC 112 ¶ 6, it is incumbent to look to the specification to identify the function and corresponding structure, which meets the limitation: "means for providing conductor portions extending from at least one upper edge to a lower edge of the edge sides of the semiconductor chips and electrically connecting the contact areas of the semiconductor chips of the semiconductor chip stack." MPEP § 2181.

Fig. 1 of the Applicant's specification and accompanying description clearly demonstrate that the "means for providing…" shall be limited to a conductive

nanoparticle-filled plastic resist. The corresponding function is to electrically connect the contact areas of the semiconductor chips of the semiconductor chip stack.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Ziskind whose telephone number is (571) 270-3397. The examiner can normally be reached on Monday thru Friday, 9-6:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Steven H. Loke can be reached on (571) 272-1657. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

DZ

/STEVEN LOKE/
Supervisory Patent Examiner, Art Unit 2818